AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) An Active load arrangement (Z) for providing ~~used to provide~~ output DC load to an object (TO) under AC test, the ~~which~~ arrangement (Z) including ~~comprises~~ a voltage controlled transistor (MOSFET) having a source (S), a gate (G) and a drain (D), wherein the ~~which~~ drain (D) is associated with the gate (G) and connected to an arrangement input (I2) associated with the object (TO), and the ~~which~~ source (S) is connected to an arrangement output (O2) associated with the object, ~~characterised by~~ the active load arrangement further comprising:

a feedback arrangement connected to the source (S) and to the gate (G), for obtaining low impedance at low frequencies and high impedance at high frequencies by the feedback arrangement ~~which feedback arrangement, by~~ varying frequency changes, phase and amplitude of the gate-to-source voltage ~~to obtain low impedance at low frequencies and high impedance at high frequencies~~.

2. (Currently Amended) The active ~~Active~~ load arrangement according to claim 1, ~~whereby~~ wherein the feedback arrangement comprises a first feedback net (FBN1) in which an inductance (L1) is connected between the source (S) and the arrangement output (O2).

3. (Currently Amended) The active ~~Active~~ load arrangement (Z) according to claim 2, ~~whereby~~ wherein the feedback arrangement comprises a second feedback net (FBN2) in which a first resistance (R1) is connected between the gate (G) and the arrangement input (I2), and a second resistance (R2) is connected between the gate (G) and the source (S), and a capacitor (C1) is connected between the gate (G) and the arrangement output (O2).

4. (Currently Amended) An active ~~Active~~ load arrangement (Z) for providing ~~used to provide~~ proper DC output load to an object (TO) under AC test, ~~which~~ the arrangement (Z) comprising ~~comprises~~ a voltage controlled transistor (MOSFET) having a source (S), a gate (G) and a drain (D), the ~~which~~ drain being ~~is~~ connected to an arrangement input (I2) associated with an output (O1) of the object (TO), whereby a first resistance (R1) is connected between the gate (G) and the drain (D), ~~*characterised in* that~~ the active load arrangement further comprising:

an inductance (L1) ~~is~~ being connected between the source (S) and an arrangement output (O2) associated with an input (I1) of the object (TO), and ~~that~~ a capacitance (C1) being ~~is~~ connected between the gate (G) and the arrangement output (O2).

5. (Currently Amended) The active ~~Active~~ load arrangement (Z) ~~used to provide proper output load to an object (TO) under test~~ according to claim 4, whereby a second resistance (R2) is connected between the gate (G) and the source (S).

6. (Currently Amended) The active ~~Active~~ load arrangement (Z) ~~used to provide proper output load to an object (TO) under test~~ according to claim 4, whereby a second resistance (R2) is connected in parallel with the capacitance (C1).

7. (Currently Amended) The active ~~Active~~ load arrangement (Z) ~~used to provide proper output load to an object (TO) under test~~ according to claim 4 ~~any of claim 4-6~~, whereby a rectifier bridge is connected ~~situated~~ between the test object (TO) and the test arrangement (TA).

8. (Currently Amended) An active ~~Active~~ load arrangement (Z1) for providing ~~used to provide~~ output load to an object (TO) under test, comprising:

~~an active load arrangement (Z) according to any of claims 1-3~~

a second active load arrangement comprising:

a voltage controlled transistor (MOSFET) having a source (S), a gate (G) and a drain (D), wherein the drain (D) is associated with the gate (G) and connected to an arrangement input (I2) associated with the object (TO), and the source (S) is connected to an arrangement output (O2) associated with the object,

the second active load arrangement further comprising a feedback arrangement connected to the source (S) and to the gate (G), for obtaining low impedance at low frequencies and high impedance at high frequencies by the feedback arrangement varying frequency changes, phase and amplitude of the gate-to-source voltage; and

a second voltage controlled transistor (MOSFET2) comprising

a second source (S2), a second gate (G2) and a second drain (D2), ~~which~~ the second source (S2) being ~~is~~ connected via the feedback arrangement to the source (S) and the gate (G) ~~and~~ via a third ~~fourth~~ resistor (R4) and a first capacitor (C1) to the second gate (G2), ~~which~~ the second gate (G2) being ~~is~~ connected via a fourth ~~fifth~~ resistance (R5) to the ~~second~~ drain (D2) and to an arrangement output (O3) associated with the test object (TO) and ~~which~~ the second gate (G2) being ~~is~~ connected to the source (S) via a second capacitor (C2).

9. (New) The active load arrangement (Z1) according to claim 8, wherein the feedback arrangement comprises a first feedback net (FBN1) in which an inductance (L1) is connected between the source (S) and the arrangement output (O2).

10. (New) The active load arrangement (Z1) according to claim 9, wherein the feedback arrangement further comprises a second feedback net (FBN2) in which a first resistance (R1) is connected between the gate (G) and the arrangement input (I2), and a second resistance (R2) is connected between the gate (G) and the source (S), and a capacitor (C1) is connected between the gate (G) and the arrangement output (O2).